

CLAIMS:

1. A VLIW processor comprising:

- a plurality of functional units;
- a distributed register file comprising a plurality of segments, the distributed register file being accessible by the functional units;
- 5 - communication means for communication with a memory;
- a communication network for coupling the functional units and the distributed register file;

characterized in that the VLIW processor further comprises spilling means for transferring data between the distributed register file and the communication means.

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2. A VLIW processor according to Claim 1 wherein:

the spilling means comprises a spill register file and a spill unit, the spill register file being accessible by the spill unit.

15 3. A VLIW processor according to Claim 1 wherein:

at least one of the segments of the distributed register file is associated with a functional unit that is unable to pass data from the segment of the distributed register file to the spilling means, a pass unit being associated with the functional unit for passing data from the segment of the distributed register file to the spilling means.

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4. A VLIW processor according to Claim 1 wherein:

the communication network comprises a partially connected communication network.

5. A VLIW processor according to Claim 3 wherein:

25 the pass unit is part of the associated functional unit.